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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,769	06/29/2001	Darren L. Abramson	42390.P10573	2024

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EXAMINER	
SPITTLE, MATTHEW D	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/896,769	ABRAMSON ET AL.	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-30* is/are allowed.

6)☒ Claim(s) *1,10,11 and 20* is/are rejected.

7)☒ Claim(s) *2-9 and 12-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 11 is directed to non-statutory intangible embodiments. In view of Applicant's disclosure, (paragraph 27), the medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., ROM, RAM, magnetic disk storage media, optical storage media, flash memory devices) and intangible embodiments (e.g., electrical, optical, acoustical, carrier waves, infrared signals, digital signals. As such, the claim is not limited to statutory subject matter and is therefore non-statutory.

Regarding claim 11, examiner suggests that applicant amend the claim to read as follows:

"A computer program product in a recordable-type media...".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garney in view of Shinomura.

Regarding claim 1, Garney teaches removing a work item of a plurality of work items from an enabled expansion bus schedule data structure (where an expansion bus schedule data structure is interpreted as a linked list; Figure 6a; column 3, line 67 – column 4, line 5; column 14, line 60 – column 15, line 2);

Generating a coherency signal independent of said work item utilizing an expansion bus host controller in response to removing said work item from said enabled expansion bus schedule data structure (where a coherency signal is interpreted as a card insertion flag; column 3, line 67 – column 4, line 5; column 14, line 60 – column 15, line 2).

Garney fails to teach reclaiming resources assigned to said work item whenever said coherency signal is generated.

Shinomura teaches a similar system where system resources are reclaimed following the removal of a work item and coherency signal being generated (column 16,

line 64 – column 17, line 12) for the purpose of allowing those resources to be re-allocated to newly added peripherals.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to reclaim resources as taught by Shinomura in the method of Garney for the purpose of allowing the said resources to be re-allocated to newly added peripherals. This would have been obvious since Shinomura teaches that system resources are limited, and must be allocated efficiently in order to effectively utilize PC cards (column 2, lines 20 – 42).

Regarding claim 10, Garney teaches the additional limitation wherein said method further comprises storing each of said plurality of work items in a memory (where a memory may be interpreted as a DEVICE DRIVER STUB RAM AREA; Figure 6a), wherein reclaiming said work item in response to generating said coherency signal comprises freeing a portion of said memory associated with said work item (where examiner interprets "the number of stub blocks within device driver stub RAM area that contains device driver stubs dynamically changes throughout the usage of the computer system as cards are added and removed" as meaning that the RAM is allocated and freed; column 10, lines 36 – 42).

* * *

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Garney in view of Shinomura, and further in view of Ritchie et al.

Regarding claim 11, Garney teaches removing a work item of a plurality of work items from an enabled expansion bus schedule data structure (where an expansion bus schedule data structure is interpreted as a linked list; Figure 6a; column 3, line 67 – column 4, line 5; column 14, line 60 – column 15, line 2);

Generating a coherency signal independent of said work item utilizing an expansion bus host controller in response to removing said work item from said enabled expansion bus schedule data structure (where a coherency signal is interpreted as a card insertion flag; column 3, line 67 – column 4, line 5; column 14, line 60 – column 15, line 2).

Garney fails to teach reclaiming resources assigned to said work item whenever said coherency signal is generated.

Shinomura teaches a similar system where system resources are reclaimed following the removal of a work item and coherency signal being generated (column 16, line 64 – column 17, line 12) for the purpose of allowing those resources to be re-allocated to newly added peripherals.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to reclaim resources as taught by Shinomura in the method of Garney for the purpose of allowing the said resources to be re-allocated to newly added peripherals. This would have been obvious since Shinomura teaches that system

resources are limited, and must be allocated efficiently in order to effectively utilize PC cards (column 2, lines 20 – 42).

Both Garney and Shinomura fail to teach the method of claim 11 embodied in a machine-readable medium that provides instructions which when executed by a machine cause said machine to perform operations.

Ritchie et al. teach that computer hardware and software are functionally interchangeable (column 5, lines 48 – 60), and that it may be preferable to have one versus the other, such as in the case of software, which enables one to modify the design more easily.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement the hardware apparatus of Garney and Shinomura in software as taught by Ritchie. This would have been obvious in order to more easily modify the design (i.e., correct errors, make functional changes, etc).

Regarding claim 20, Garney teaches the additional limitation wherein said method further comprises storing each of said plurality of work items in a memory (where a memory may be interpreted as a DEVICE DRIVER STUB RAM AREA; Figure 6a), wherein reclaiming said work item in response to generating said coherency signal comprises freeing a portion of said memory associated with said work item (where examiner interprets "the number of stub blocks within device driver stub RAM area that contains device driver stubs dynamically changes throughout the usage of the computer

system as cards are added and removed" as meaning that the RAM is allocated and freed; column 10, lines 36 – 42).

Allowable Subject Matter

Claims 2 – 9, and 12 – 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 21 – 30 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claim 21, the limitation **a status register including a status signal bit to notify an expansion bus host controller driver that resources assigned to said work item may be reclaimed**, when read within the remainder of the claim, makes claim 14 allowable over the prior art. Claims 22 – 26 are allowed based up on their dependence to claim 21.

Regarding claim 27, the limitation **a processor to remove a work item of said plurality of work items from said expansion bus schedule data structure, to modify said command signal bit in response to said removal of said work item from said expansion bus schedule data structure; and to reclaim resources assigned to said work item in response to a modification of said status bit**, when

read within the remainder of the claim, makes claim 27 allowable over the prior art. Claims 28 – 30 are allowed based upon their dependence to claim 27.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Cottingham can be reached on 571-272-7079. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JOHN R. COTTINGHAM
PRIMARY EXAMINER